



# Overvoltage-Protection Controller with USB ESD Protection

## General Description

The MAX4987AE/MAX4987BE are overvoltage protection devices with built-in ESD protection for USB data lines. These devices feature a low 100mΩ (typ) R<sub>ON</sub> internal nFET switch and protect low-voltage systems against voltage faults up to +28V. When the input voltage exceeds the overvoltage threshold or decreases below the undervoltage threshold, the internal nFET switch is turned off to prevent damage to the protected components.

All switches feature a minimum 1.5A current-limit protection. During a short-circuit occurrence, the switch operates in an autoretry mode where the internal nFET switch is turned on to check if the fault has been removed. The autoretry interval is 30ms, and if the fault is removed, the nFET switch remains on.

The MAX4987AE/MAX4987BE feature low-capacitance (3pF) ESD protection for USB data lines that allow transmission of high-speed USB 2.0 signals.

The overvoltage threshold (OVLO) is preset to 6.15V. The undervoltage thresholds (UVLO) are preset to 2.55V (MAX4987AE) or 4.2V (MAX4987BE). When the input voltage drops below the undervoltage (UVLO) threshold, the devices enter a low-current standby mode.

All devices are offered in a small 2mm x 3mm, 8-pin TDFN package and operate over the -40°C to +85°C extended temperature range.

## Applications

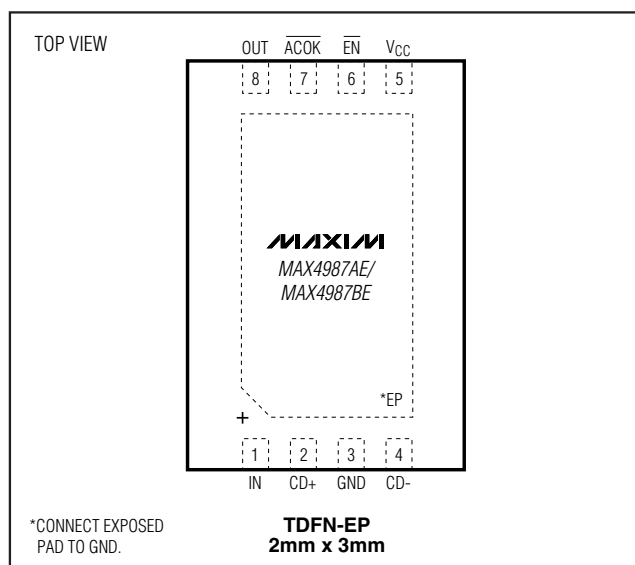
Cell Phones  
Media Players

*Typical Operating Circuit appears at end of data sheet.*

## Features

- ◆ Input Voltage Protection Up to +28V
- ◆ Integrated Low R<sub>ON</sub> (100mΩ) nFET Switch
- ◆ Internal Overcurrent Protection 1.5A (min)
- ◆ Overcurrent Protection (Autoretry)
- ◆ Enable Input
- ◆ Internal 30ms Startup Delay
- ◆ Low-Capacitance USB High-Speed Data Line ESD Protection (3pF)
  - ±15kV Human Body Model
  - ±15kV IEC 61000-4-2 Air Gap
  - ±6kV IEC 61000-4-2 Contact
- ◆ Thermal-Shutdown Protection
- ◆ 2mm x 3mm, 8-Pin TDFN Package

## Pin Configuration



MAX4987AE/MAX4987BE

## Ordering Information/Selector Guide

PART	PIN-PACKAGE	TOP MARK	PACKAGE CODE	UVLO (V)	OVLO (V)	OVERCURRENT MODE
MAX4987AEETA+	8 TDFN-EP**	AAI	T823-1	2.55	6.15	Autoretry
MAX4987BEETA+*	8 TDFN-EP**	AAJ	T823-1	4.2	6.15	Autoretry

**Note:** All devices are specified over the -40°C to +85°C operating temperature range.

+ Denotes a lead-free package.

\* Future product—contact factory for availability.

\*\* EP = Exposed paddle.



# Overvoltage-Protection Controller with USB ESD Protection

## ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

IN	-0.3V to +30V
OUT	-0.3V to +(IN + 0.3V)
V <sub>CC</sub> , $\overline{\text{EN}}$ , $\overline{\text{ACOK}}$ , CD+, CD-	-0.3V to +6V
Continuous Power Dissipation (T <sub>A</sub> = +70°C) for multilayer board: 8-Pin TDFN (derate 16.7mW/°C above +70°C)	1333mW
Package Junction-to-Ambient Thermal Resistance ( $\theta_{\text{JA}}$ ) (Note 1)	60.0°C/W

Package Junction-to-Case Thermal Resistance ( $\theta_{\text{JC}}$ ) (Note 1)	10.8°C/W
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering)	+300°C

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, go to [www.maxim-ic.com/thermal-tutorial](http://www.maxim-ic.com/thermal-tutorial).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>IN</sub> = +2.2V to +28V, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at V<sub>IN</sub> = +5V and T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	
<b>ANALOG SWITCH</b>							
Input-Voltage Range	V <sub>IN</sub>		2.2		28	V	
V <sub>CC</sub> Input Voltage	V <sub>CC</sub>				5.5	V	
Input Supply Current	I <sub>IN</sub>	$\overline{\text{EN}} = 0\text{V}$ , V <sub>IN</sub> > V <sub>UVLO</sub>		60	150	μA	
		$\overline{\text{EN}} = 5\text{V}$ , V <sub>IN</sub> > V <sub>UVLO</sub>		50	100		
UVLO Supply Current	I <sub>UVLO</sub>	V <sub>IN</sub> < V <sub>UVLO</sub>			40	μA	
IN Undervoltage Lockout	V <sub>UVLO</sub>	(V <sub>IN</sub> falling)	MAX4987AE	2.3		V	
			MAX4987BE	3.8			
		(V <sub>IN</sub> rising)	MAX4987AE	2.35	2.55		2.75
			MAX4987BE	3.85	4.2		4.45
IN Undervoltage Lockout Hysteresis			1		%		
Overvoltage Trip Level	V <sub>OVLO</sub>	(V <sub>IN</sub> rising)	5.55	6.15	6.45	V	
		(V <sub>IN</sub> falling)	5.5				
IN Overvoltage Lockout Hysteresis			1		%		
Switch On-Resistance	R <sub>ON</sub>	V <sub>IN</sub> = 5V, I <sub>OUT</sub> = 500mA		100	200	mΩ	
Overcurrent Protection Threshold	I <sub>LIM</sub>		1.5		4.2	A	
Maximum Output Capacitance		V <sub>IN</sub> = 5V, no overcurrent shutdown		1000		μF	
CD+ and CD- Leakage Current	I <sub>LKG_CD</sub>	V <sub>CC</sub> = 5.5V, V <sub>CD-</sub> = 0V, 3.3V	-300		+300	nA	
CD+ and CD- Capacitance	C <sub>CD</sub>	f = 1MHz, V <sub>CD-</sub> = 0.5p-p		3		pF	
<b>DIGITAL SIGNALS</b>							
$\overline{\text{ACOK}}$ Output Low Voltage	V <sub>OL</sub>	I <sub>SINK</sub> = 1mA			0.4	V	
$\overline{\text{ACOK}}$ High-Leakage Current		V <sub><math>\overline{\text{ACOK}}</math></sub> = 5.5V, flag deasserted			1	μA	
$\overline{\text{EN}}$ Input-Voltage High	V <sub>IH</sub>		1.4			V	
$\overline{\text{EN}}$ Input-Voltage Low	V <sub>IL</sub>				0.4	V	
$\overline{\text{EN}}$ Input-Leakage Current	I <sub>LEAK</sub>	V <sub>EN</sub> = 5.5V	-1		+1	μA	

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MAX4987AE/MAX4987BE

## ELECTRICAL CHARACTERISTICS (continued)

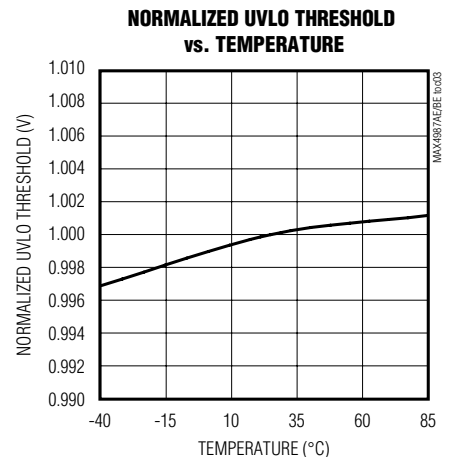
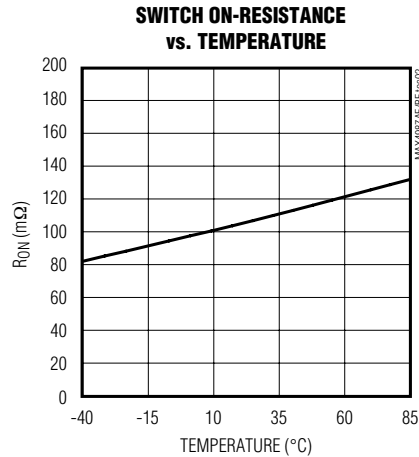
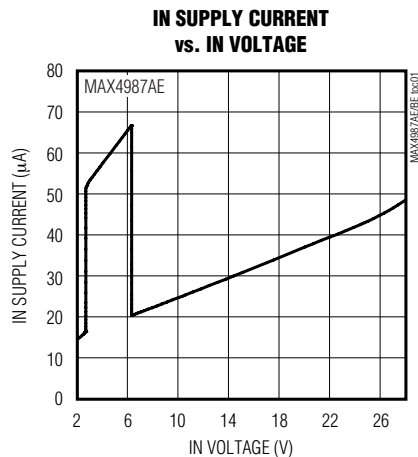
( $V_{IN} = +2.2V$  to  $+28V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{IN} = +5V$  and  $T_A = +25^{\circ}C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
<b>TIMING CHARACTERISTICS (Note 2)</b>						
Debounce Time	$t_{INDBC}$	Time from $V_{UVLO} < V_{IN} < V_{OVLO}$ to charge-pump enable		30		ms
$\overline{ACOK}$ Assertion Time	$t_{ACOK}$	$V_{UVLO} < V_{IN} < V_{OVLO}$ , to $\overline{ACOK}$ low		30		ms
Switch Turn-On Time	$t_{ON}$	$V_{UVLO} < V_{IN} < V_{OVLO}$ , $R_{LOAD} = 100\Omega$ , from 10% to 90% of $V_{OUT}$		3		ms
Switch Turn-Off Time	$t_{OFF}$	$V_{IN} < V_{UVLO}$ or $V_{IN} > V_{OVLO}$ to internal switch off, $R_{LOAD} = 100\Omega$			10	$\mu s$
Current-Limit Turn-Off Time	$t_{BLANK}$	Overcurrent fault to internal switch off		10		$\mu s$
Autoretry Time	$t_{RETRY}$	From overcurrent fault to internal switch turn-on		30		ms
<b>THERMAL PROTECTION</b>						
Thermal Shutdown	$T_{SHDN}$			150		$^{\circ}C$
Thermal-Shutdown Hysteresis				40		$^{\circ}C$
<b>ESD PROTECTION</b>						
CD+ and CD-		Human Body Model		$\pm 15$		kV
		IEC 61000-4-2 Air Gap		$\pm 15$		
		IEC 61000-4-2 Contact		$\pm 6$		
All Other Pins		Human Body Model		$\pm 2$		kV

**Note 2:** All timing is specified using 20% and 80% levels, unless otherwise noted.

## Typical Operating Characteristics

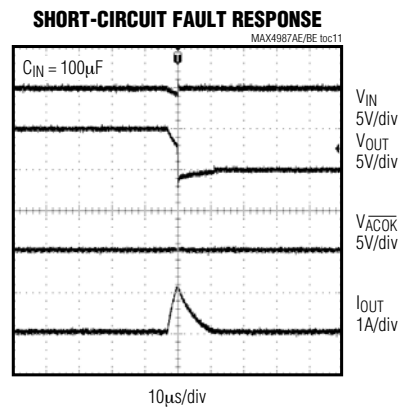
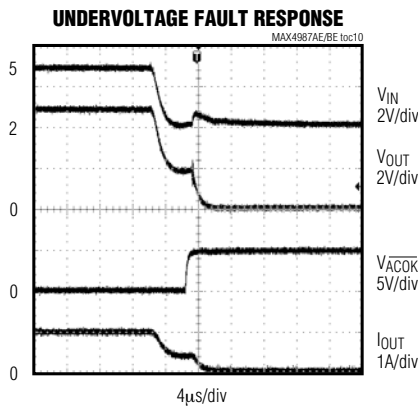
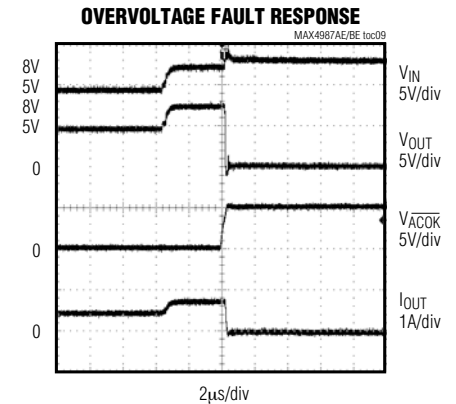
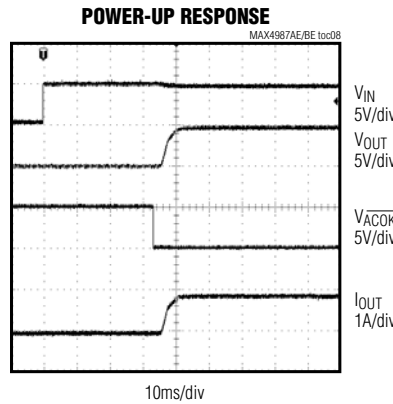
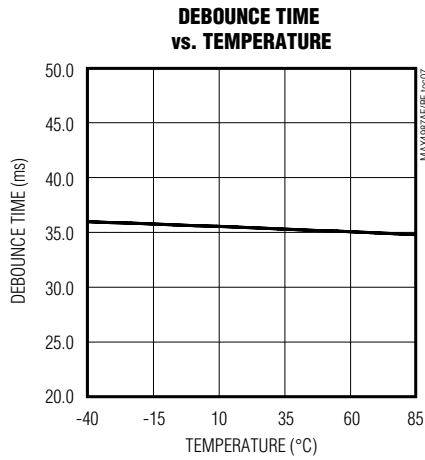
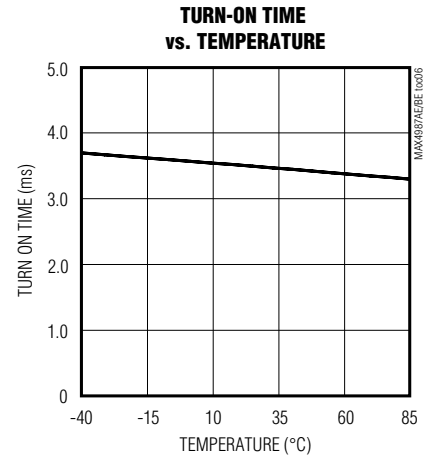
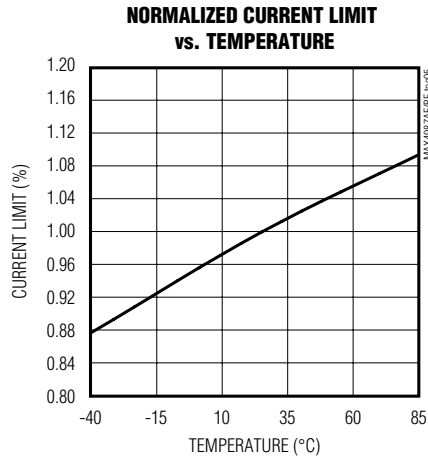
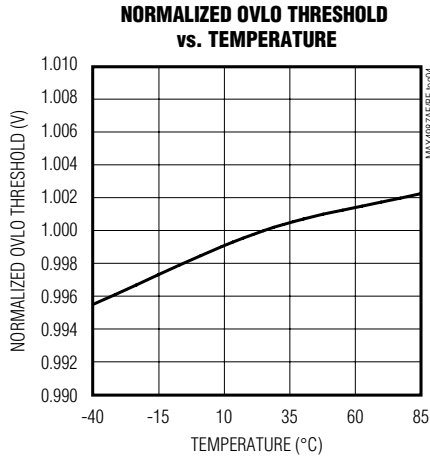
( $T_A = +25^{\circ}C$ , unless otherwise noted.)



# Overvoltage-Protection Controller with USB ESD Protection

## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

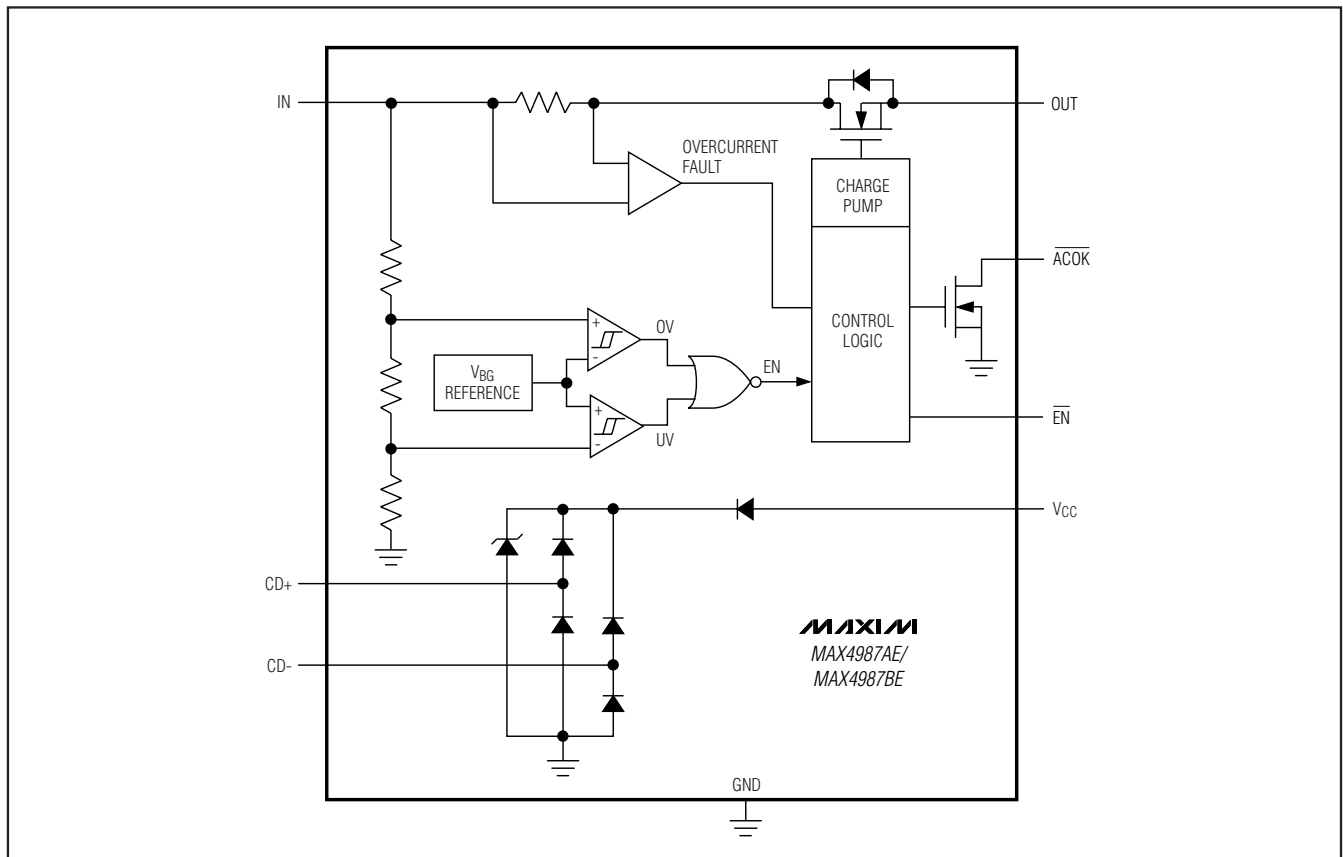


# Overvoltage-Protection Controller with USB ESD Protection

## Pin Description

PIN	NAME	FUNCTION
1	IN	Voltage Input. Bypass IN with a 1 $\mu$ F ceramic capacitor as close to the device as possible to obtain $\pm$ 15kV HBM ESD protection. No capacitor required to obtain $\pm$ 2kV HBM ESD protection.
2	CD+	USB Data Line
3	GND	Ground
4	CD-	USB Data Line
5	VCC	Positive Supply-Voltage Input. VCC is required only when USB signals are present.
6	$\overline{\text{EN}}$	Enable Active-Low Input. Drive $\overline{\text{EN}}$ low to enable the switch. Drive $\overline{\text{EN}}$ high to disable the switch.
7	$\overline{\text{ACOK}}$	Open-Drain Adapter-Voltage Indicator Output. $\overline{\text{ACOK}}$ is driven low after the V <sub>IN</sub> voltage is stable between UVLO and OVLO for 30ms (typ). Connect a pullup resistor from $\overline{\text{ACOK}}$ to the logic I/O voltage of the host system.
8	OUT	Output Voltage. Output of internal switch.
EP	EP	Exposed Pad. Connect exposed pad to ground. Do not use EP as a sole ground connection.

## Functional Diagram



MAX4987AE/MAX4987BE

# Overvoltage-Protection Controller with USB ESD Protection

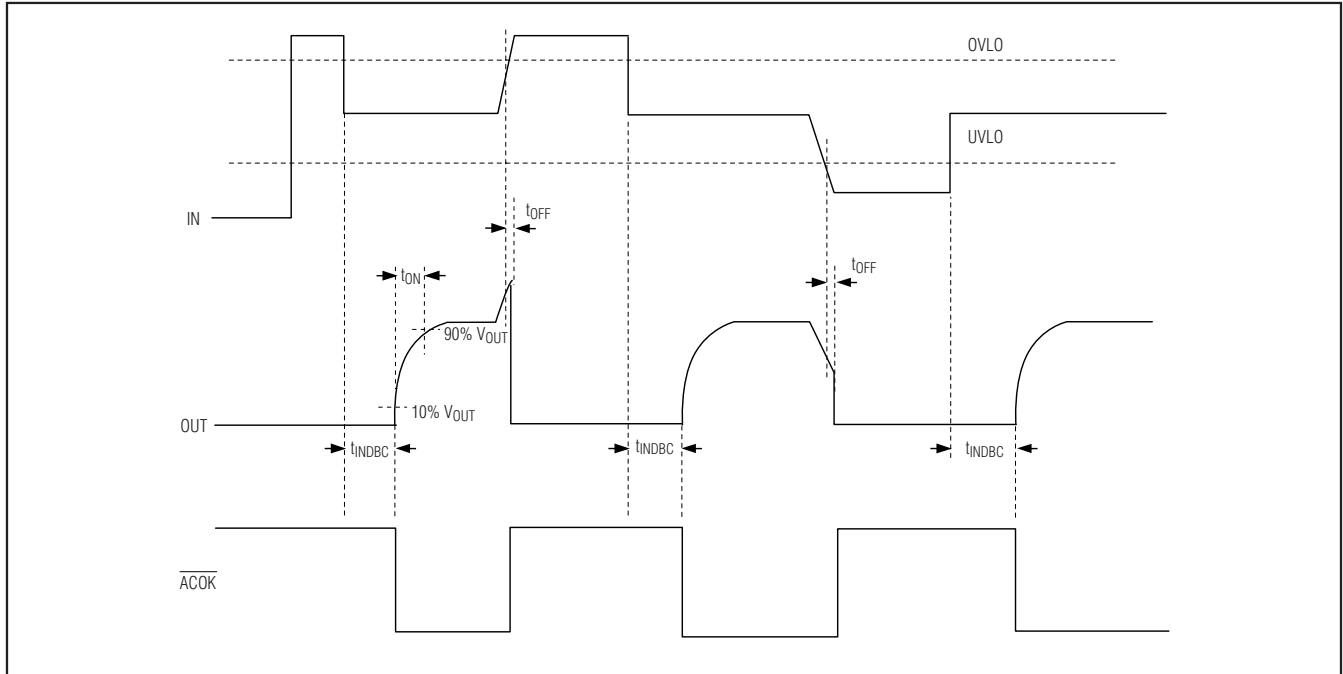


Figure 1. MAX4987AE/MAX4987BE Timing Diagram

## Detailed Description

The MAX4987AE/MAX4987BE are overvoltage protection devices with integrated ESD protection for USB data lines. These devices feature a low  $R_{ON}$  internal FET and protect low-voltage systems against voltage faults up to +28V. If the input voltage exceeds the overvoltage threshold, the internal nFET switch is turned off to prevent damage to the protected components. The 30ms debounce time prevents false turn-on of the internal nFET switch during startup. An open-drain active-low logic output is available to signal that a successful power-up has occurred.

### Device Operation

The MAX4987AE/MAX4987BE have an internal oscillator and charge pump that control the turn-on of the internal nFET switch. The internal oscillator controls the timers that enable the turn-on of the charge pump and controls the state of the open-drain  $\overline{ACOK}$  output. If  $V_{IN} < V_{UVLO}$  or if  $V_{IN} > V_{OVLO}$ , the internal oscillator remains off, thus disabling the charge pump. If  $V_{UVLO} < V_{IN} < V_{OVLO}$ , the internal charge pump is enabled. The charge-pump startup, after a 30ms internal delay, turns on the internal nFET switch and asserts  $\overline{ACOK}$  (see Figure 1). At any time, if  $V_{IN}$  drops below  $V_{UVLO}$  or rises above  $V_{OVLO}$ ,  $\overline{ACOK}$  is pulled high and the charge pump is disabled.

## Internal nFET Switch

The MAX4987AE/MAX4987BE incorporate an internal nFET switch with a  $100\text{m}\Omega$  (typ) on-resistance. The nFET switch is internally driven by a charge pump that generates a voltage above the input voltage. The MAX4987AE/MAX4987BE is equipped with a 1.5A (min) current-limit protection that turns off the nFET switch within  $5\mu\text{s}$  (typ) during an overcurrent fault condition.

### Autoretry

The MAX4987AE/MAX4987BE have an overcurrent autoretry function that turns on the nFET switch again after a 30ms (typ) retry time (see Figure 2). If the faulty load condition is still present after the blanking time, the switch turns off again and the cycle is repeated. The fast turn-off time and 30ms retry time result in a very low duty cycle in order to keep power consumption low. If the faulty load condition is not present, the switch remains on.

### Undervoltage Lockout (UVLO)

The MAX4987AE has a 2.55V undervoltage-lockout threshold (UVLO), while the MAX4987BE has a 4.15V UVLO threshold. When  $V_{IN}$  is less than  $V_{UVLO}$ ,  $\overline{ACOK}$  is high impedance.

# Overvoltage-Protection Controller with USB ESD Protection

MAX4987AE/MAX4987BE

## Overvoltage Lockout (OVLO)

The MAX4987AE/MAX4987BE have a 6.15V (typ) overvoltage threshold (OVLO). When  $V_{IN}$  is greater than  $V_{OVLO}$ ,  $\overline{ACOK}$  is high impedance.

## ACOK

$\overline{ACOK}$  is an active-low open-drain output that asserts low when  $V_{UVLO} < V_{IN} < V_{OVLO}$  following the 30ms (typ) debounce period. Connect a pullup resistor from  $\overline{ACOK}$  to the logic I/O voltage of the host system. During a short-circuit fault,  $\overline{ACOK}$  may deassert due to  $V_{IN}$  not being in the valid operating voltage range.

## Thermal-Shutdown Protection

The MAX4987AE/MAX4987BE feature thermal-shutdown circuitry. The internal nFET switch turns off when the junction temperature exceeds  $T_{SHDN}$  and immediately goes into a fault mode. The device exits thermal shutdown after the junction temperature cools by +40°C (typ).

## Applications Information

### IN Bypass Capacitor

For most applications, bypass IN to GND with a 1 $\mu$ F ceramic capacitor as close to the device as possible to enable  $\pm 15$ kV HBM ESD protection on IN. If  $\pm 15$ kV HBM ESD protection is not required, there is no capacitor required at IN. If the power source has significant inductance due to long lead length, take care to prevent overshoots due to the LC tank circuit and provide protection if necessary to prevent exceeding the absolute maximum rating on IN.

### ESD Test Conditions

ESD performance depends on a number of conditions. The MAX4987AE/MAX4987BE are specified for  $\pm 15$ kV HBM ESD protection on the CD+, CD-, and IN pins when IN is bypassed to ground with a 1 $\mu$ F ceramic capacitor. The CD+ and CD- inputs are also protected against  $\pm 15$ kV Air Gap and  $\pm 6$ kV contact IEC 61000-4-2 ESD events.

### Human Body Model

Figure 3 shows the Human Body Model, and Figure 4 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, that is then discharged into the device through a 1.5k $\Omega$  resistor.

### IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The MAX4987AE/ MAX4987BE

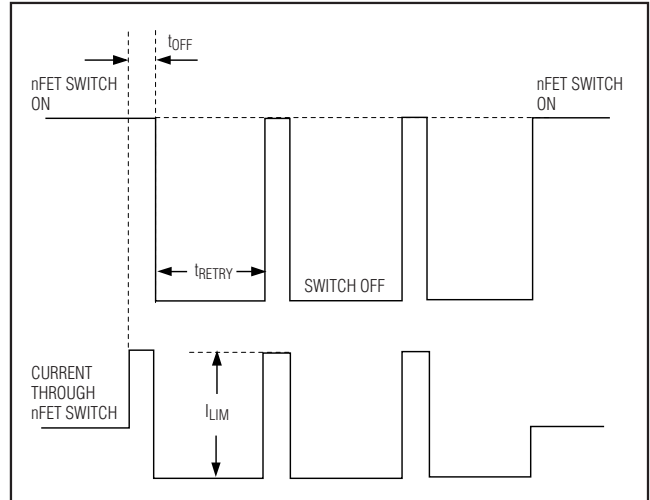


Figure 2. Autoretry Timing Diagram

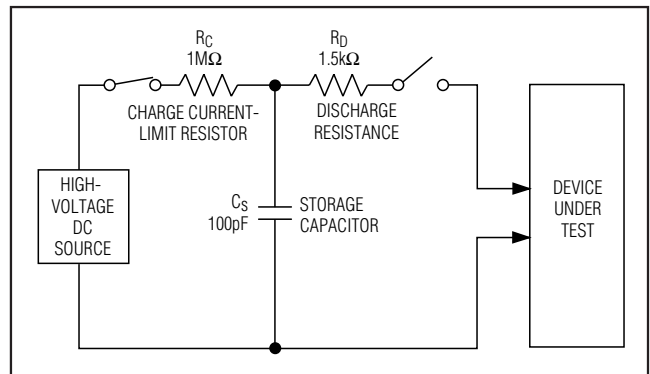


Figure 3. Human Body ESD Test Model

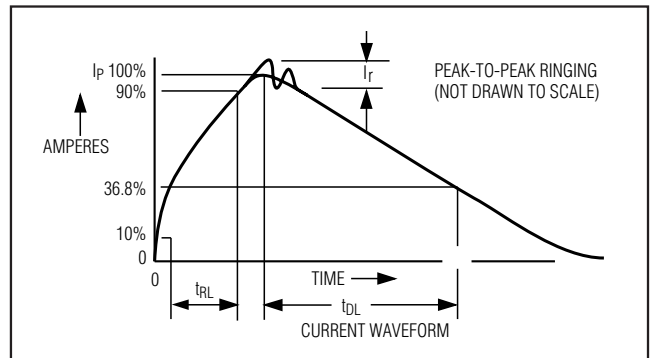


Figure 4. Human Body Current Waveform

# Overvoltage-Protection Controller with USB ESD Protection

are specified for  $\pm 15\text{kV}$  Air-Gap Discharge and  $\pm 6\text{kV}$  Contact Discharge IEC 61000-4-2 on the CD+ and CD- pins.

The major difference between tests done using the Human Body Model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2, due to lower series resistance. Hence, the ESD withstand voltage measured to IEC 61000-4-2 generally is lower than that measured using the Human Body Model. Figure 5 shows the IEC 61000-4-2 model. The Contact Discharge method connects the probe to the device before the probe is charged. The Air-Gap Discharge test involves approaching the device with a charged probe.

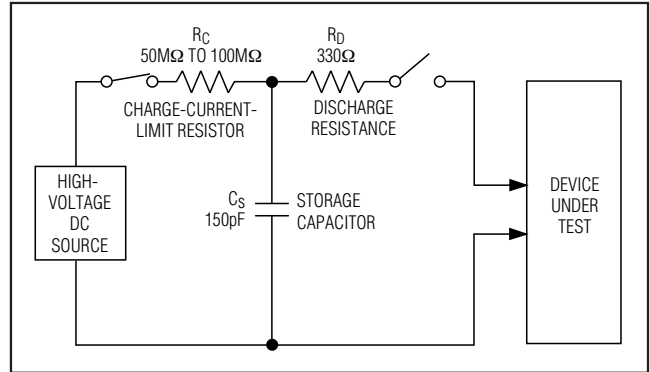
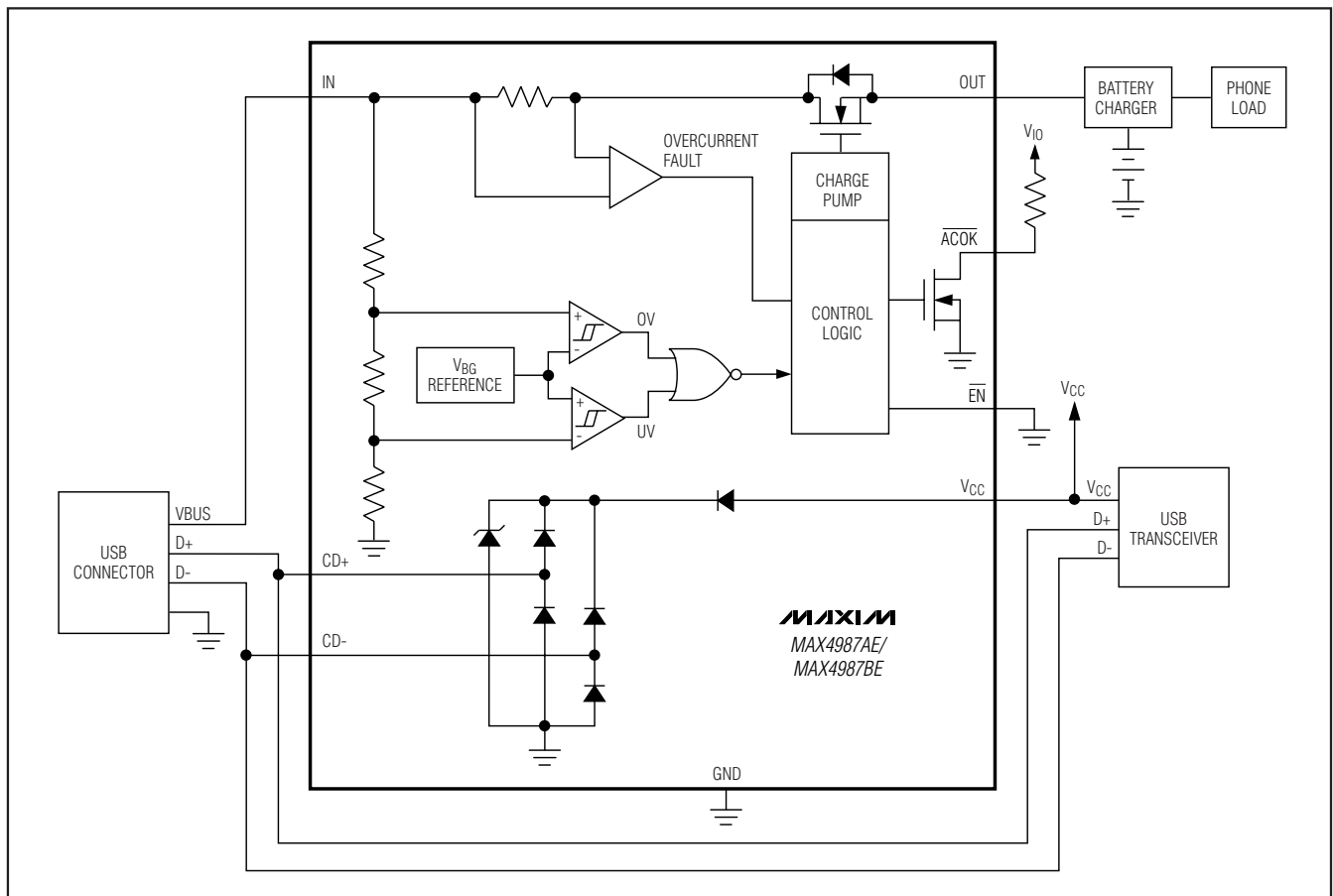


Figure 5. IEC 61000-4-2 ESD Test Model

## Typical Operating Circuit



## Chip Information

PROCESS: BiCMOS

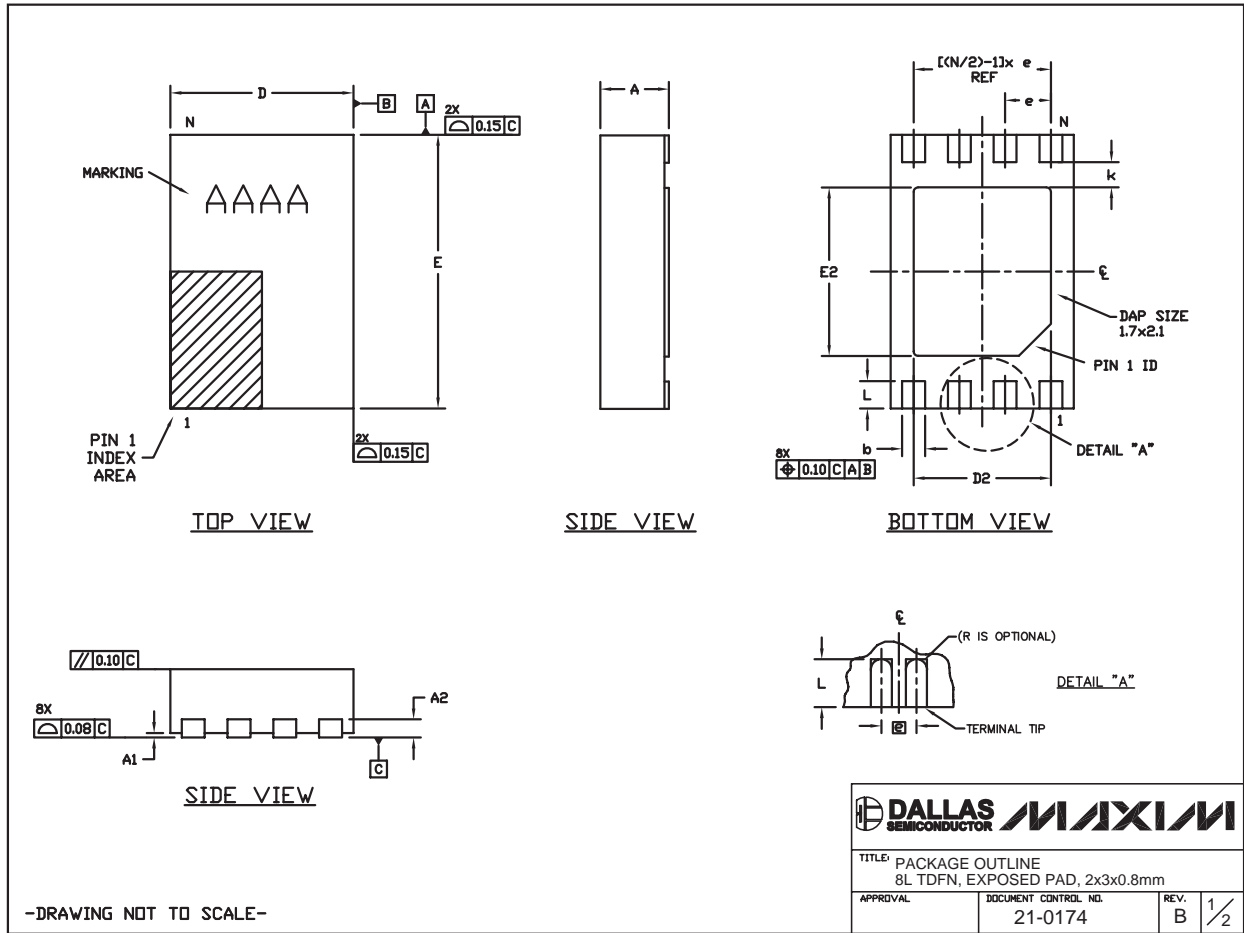


# Overvoltage-Protection Controller with USB ESD Protection

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX4987AE/MAX4987BE



# Overvoltage-Protection Controller with USB ESD Protection

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

DIMENSIONS			
SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
E	2.95	3.00	3.05
D	1.95	2.00	2.05
A1	0.00	0.02	0.05
L	0.30	0.40	0.50
k	0.20 MIN.		
A2	0.20 REF.		
N	8		
e	0.50 BSC		
b	0.18	0.25	0.30

EXPOSED PAD PACKAGE						
PKG. CODE	E2			D2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T823-1	1.60	1.75	1.90	1.50	1.63	1.75

**NOTES:**

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.  
COPLANARITY SHALL NOT EXCEED 0.08mm.
3. WARPAGE SHALL NOT EXCEED 0.10mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. COMPLY TO JEDEC MO229, TYPE 1, VERSION WCED-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC #10-0131.

-DRAWING NOT TO SCALE-

			
TITLE: PACKAGE OUTLINE 8L TDFN, EXPOSED PAD, 2x3x0.8mm			
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0174	B	2/2

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